REMARKS

Applicant hereby traverses the rejections of record and requests reconsideration and withdrawal of such in view of the remarks contained herein. Claims 1-17 are pending in this application.

Rejection Under 35 U.S.C. 112(1)

Claims 1-4 and 12 are rejected under 35 U.S.C. 112, first paragraph, for failing to comply with the enablement requirement. As Applicant best understands, Examiner believes "monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge..." as recited in claim 1 does not satisfy the enablement requirement. The Examiner opines that, according to the specification, "monitoring a TLB purge operation is implemented in *both* [and only *both*] software and hardware." *See* Current Action, paragraph 5 (emphasis added). As an initial matter, Applicant respectfully asserts that the Examiner has not established a prima facie case of lack of enablement. In order to make a rejection, the Examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. *In re Wright*, 999 F.2d 1557, 1562 (Fed. Cir. 1993) (examiner must provide a reasonable explanation as to why the scope of protection provided by a claim is not adequately enabled by the disclosure). In the case at hand, Examiner points to pgs. 1, 10, 11, 18, and 38-39 of the specification to support the rejection. *See* Current Action, paragraph 5. However, in doing so, the Examiner has mischaracterized the specification through paraphrasing and improper context. For example, the Examiner's reference to pgs. 38-39 of the specification does not mention TLB monitoring. Applicant respectfully disagrees with the Examiner's apparent understanding of the specification and maintains that the claims are enabled.

In support of enablement, Applicant directs the Examiner's attention to the Abstract, which recites "The invention monitors and detects Translation Lookaside Buffer ("TLB") purges, a hardware-based operation..." (emphasis added). Applicant further directs the Examiner's attention to pg. 44 lines 15-17, which recites "The foregoing discussion also discloses the basis for additional novelty in data copy operations by monitoring for TLB purges during the operation itself while it is being performed by hardware." (emphasis

added). In view of the above, Applicant submits that the specification enables monitoring, as a hardware operation, for an occurrence of a TLB purge.

Moreover, as the Examiner has noted, at pg. 1 lines 5-7, the specification recites "The invention is operable in an environment in which data movement is performed largely by hardware rather than software, and is enabled responsive to monitoring and detection of Translation Lookaside Buffer ("TLB") purges." As the Applicant has noted, one of ordinary skill in the art would understand that certain embodiments of the invention operate in environments in which data movement is performed largely by hardware and/or environments in which data movement is provided entirely by hardware. This notion is further supported where the specification recites "the claimed invention operates when aspects of data movement are enabled in hardware rather than software..." *See* pg. 13, lines 7-9 (emphasis added). Support is also found where the specification recites "the claimed invention is operable...by performing operation integral to data movement, such as memory allocation and notification, with hardware rather than software." *See* pg. 10, lines 1-5 (emphasis added).

Rejection Under 35 U.S.C. 102(e)

Claims 1, 4, and 12 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,906,001 to Wu et al (hereinafter "Wu").

"It is well settled that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ.2d 1051, 1053 (Fed. Cir. 1987). Appellant respectfully asserts that Wu does not teach each and every element of each of claims 1, 4, and 12, and accordingly does not meet the *Verdegaal* requirements.

Claim 1 recites "monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory." The Examiner states that Wu teaches the recited element at col. 2, lines 33-54. *See* Current Action, paragraph 7. However, at the Examiner's citation

Wu merely describes methods of maintaining coherency among several caches. Wu teaches "snooping" for maintaining coherency in data caches. *See* col. 2, lines 42-44. Wu also teaches that "while snooping is commonly used to maintain coherency in data caches, it is typically not employed for maintaining TLB coherency." *Id.* Wu further teaches a TLB "shootdown" operation. *See* col. 2, line 45-col. 3, line 11. However, the shootdown operation of Wu appears to be a software-based operation. For example, the shootdown operation executes an INVPLG instruction that is used by an operating system or software routine. *See* col. 2, lines 19-29. The shootdown operation may also use a software interrupt instruction, INT. *See* col. 2, lines 64-11. As such, these methods do not teach monitoring, as a hardware operation, for an occurrence of a TLB purge during setup and execution of a data movement operation from virtual memory. Accordingly, Wu does not teach "monitoring, as a hardware operation, for an occurrence of a translation lookaside buffer (TLB) purge during setup and execution of a data movement operation from virtual memory" as recited in claim 1. Thus, Wu does not anticipate claim 1.

Claims 4 and 12 depend directly from claim 1. Because claims 4 and 12 depend directly from claim 1, they contain all elements of the base claim. As shown above, Wu does not teach all elements of claim 1. Accordingly, Wu does not teach all elements of claims 4 and 12. Thus, Wu does not anticipate claims 4 and 12. Appellant respectfully requests that the rejection of record be withdrawn and claims 1, 4, and 12 passed to allowance.

Double Patenting Rejection

Claims 1-17 are rejected under the judicially-created doctrine of double patenting over claims 1-10 of U.S. Patent No. 6,668, 314 to Brewer (hereinafter "*Brewer* '314"). Claims 6-11 and 15-17 are rejected under the judicially-created doctrine of double patenting over claims 12-16 of U.S. Patent No. U.S. Patent No. 5,966,733 to Brewer (hereinafter *Brewer* '733"). Applicant again proposes filing a terminal disclaimer in compliance with 37 C.F.R. § 1.321(b) if the Examiner's rejection still properly stands after an indication of allowability over prior art of record in the present case.

Conclusion

Applicant believes the pending application is in condition for allowance. Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 08-2025, under Order No. 10970696-3 from which the undersigned is authorized to draw.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as Express Mail, Airbill No. EV568255121US in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: April 4, 2006

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Respectfully submitted,

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